AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor apparatus including a MOS-type device, comprising:

a first switch ~~for supplying~~ configured to supply a gate current during a first turn-on operation for turning on ~~the gate of~~ said MOS-type device;

a second switch ~~for discharging~~ configured to discharge a gate capacitance during a turn-off operation for turning off ~~the gate of~~ said MOS-type device;

a third switch ~~for increasing~~ configured to increase said gate current;

first timer ~~means for turning~~ configured to turn on said third switch in conjunction with the turn-on of said first switch, and then configured to turn ~~turning~~ off said third switch after a first predetermined time from said turn-on of said third switch;

a fourth switch configured to increase ~~for increasing~~ the discharge current during said ~~gate~~ turn-off operation; and

second timer ~~means~~ configured to turn ~~for turning~~ on said fourth switch in conjunction with the turn-on of said second switch, and then configured to turn ~~turning~~ off said fourth switch after a second predetermined time from said turn-on of said fourth switch.

Claim 2 (Currently Amended): The semiconductor apparatus as defined in claim 1, wherein the first and third switches form a first gate turn-on circuit, further comprising ~~which includes~~:

a second gate turn-on circuit connected in parallel with said first gate turn-on circuit and configured to perform a second turn-on operation ~~other than a first gate turn-on circuit having said first and third switches~~; and

means for detecting a collector current of said MOS-type device,

wherein when said detected collector current is less than a predetermined value, only said first gate turn-on circuit is activated to provide the gate current at a first amount, and

when said detected collector current is equal to or greater than said predetermined value, both said first and second gate turn-on circuits are activated to provide the gate current at a second amount greater than said first amount.

Claim 3 (Currently Amended): The semiconductor apparatus as defined in claim 2, wherein when the detected collector current of said MOS-type device which is turned on ~~according to a~~ after the first turn-on operation is equal to or greater than said predetermined value, said second gate turn-on circuit is activated to perform the ~~in a~~ second turn-on operation subsequent to said first turn-on operation.

Claim 4 (Currently Amended): The semiconductor apparatus as defined in claim 1, wherein said first predetermined time is set at a value configured to allow ~~allowing~~ said MOS-type device to be turned on after said first and third switches are turned on, and said second predetermined time is set at a value configured to allow ~~allowing~~ said MOS-type device to be turned off after said second and fourth switches are turned on.

Claim 5 (New): The semiconductor apparatus as defined in claim 1, wherein said third switch is connected in parallel to a first constant current device.

Claim 6 (New): The semiconductor apparatus as defined in claim 1, wherein said first and third switches are connected in series.

Claim 7 (New): The semiconductor apparatus as defined in claim 1, wherein said second switch is connected in series to a second constant current device and said fourth switch is connected in series to a third constant current device, and the second switch with the second constant current device is connected in parallel to the fourth switch with the third constant current device.

Claim 8 (New): The semiconductor apparatus as defined in claim 1, wherein the second switch is connected between the gate and an emitter of the MOS-type device through a second constant current device, and the fourth switch is connected between the gate and the emitter of the MOS-type device through a third constant current device.

Claim 9 (New): The semiconductor apparatus as defined in claim 2, wherein said first and second gate turn-on circuits are connected between a power supply voltage and the gate of said MOS-type device.